CLAIMS

What is claimed is:

1. A voltage regulator, comprising:

an error amplifier that amplifies a voltage difference between a reference voltage and a sampled output voltage of the voltage regulator;

a driver amplifier that receives said amplified voltage difference and that produces a gate driving voltage;

an output transistor that has a gate that receives said gate driving voltage and a source that outputs a regulated output voltage;

a Miller compensation capacitor that feeds a sample of said regulated output voltage back to an input of said driver amplifier; and

an Ahuja compensation circuit that feeds a portion of said regulated output voltage back to said input of said driver amplifier.

2. The voltage regulator of Claim 1 wherein a zero resulting from said Miller compensation capacitor at least partially cancels a pole resulting from said Ahuja compensation circuit.

3. The voltage regulator of Claim 2 wherein said zero produced by said Miller compensation capacitor tracks said pole produced by said Ahuja compensation circuit.

4. The voltage regulator of Claim 2 wherein a frequency of said zero produced by said Miller compensation capacitor is within a capacitive gain factor of a frequency of said pole produced by said Ahuja compensation circuit.

5. The voltage regulator of Claim 2 wherein said Ahuja compensation circuit includes an Ahuja feedback capacitor, and wherein a ratio of said Ahuja feedback capacitor and said Miller compensation capacitor is less than about 3.

6. The voltage regulator of Claim 1 wherein said driver amplifier has an output impedance of between about 100Ω and 200Ω.

7. The voltage regulator of Claim 1 wherein said driver amplifier comprises a plurality of series-connected amplifiers.

8. The voltage regulator of Claim 7 wherein said driver amplifier comprises four series-connected amplifiers.

9. The voltage regulator of Claim 8 wherein said voltage regulator having at least two nested feedback paths.

10. The voltage regulator of Claim 1 wherein said error amplifier comprises a P-channel input differential pair amplifier.

11. The voltage regulator of Claim 1 wherein said output transistor is a power P-channel MOSFET.

12. The voltage regulator of Claim 4 wherein said Ahuja compensation circuit includes an Ahuja feedback capacitor and wherein said capacitive gain factor is equal to one plus a ratio of a value of said Ahuja feedback capacitor divided by a value of said Miller compensation capacitor.

13. A voltage regulator apparatus comprising:

an outer loop including an error amplifier having an output that communicates with an input of a driver amplifier, a regulated voltage output responsive to an output of said driver amplifier, and an outer feedback path from said regulated voltage output to an input of said error amplifier that maintains said regulated voltage output based on a reference voltage;

an inner loop including a first feedback path and a second feedback path around said driver amplifier, wherein said first and second feedback paths do not include said error amplifier, and wherein a zero produced by said first feedback path at least partially cancels, in said inner loop, a pole produced by said second feedback path.

14. The voltage regulator apparatus of Claim 13 wherein said first feedback path includes a Miller compensation capacitor (C_m) and said second feedback path includes an Ahuja compensation circuit.

15. The voltage regulator of Claim 14 wherein said Ahuja compensation circuit includes an Ahuja feedback capacitor (C_a), and wherein a ratio of said Ahuja feedback capacitor and said Miller compensation capacitor is less than about 3.

16. The voltage regulator of Claim 15 wherein said pole and said zero are within a capacitive gain factor of (1+Ca/Cm).

17. A method for regulating voltage comprising:

comparing a sampled DC voltage to a reference voltage to generate a correction signal;

amplifying the correction signal utilizing a driver amplifier;

generating a regulated output voltage based on said amplified correction signal, wherein said sampled DC voltage is related to said regulated output voltage;

feeding back said regulated output voltage to said driver amplifier utilizing Miller compensation; and

feeding back said regulated output voltage to said driver amplifier utilizing Ahuja compensation.

18. The method of Claim 17 further comprising selecting a Miller compensation capacitor (C_m) and an Ahuja feedback capacitor (C_a) so that a zero resulting from said Miller compensation capacitor at least partially cancels a pole resulting from said Ahuja feedback capacitor.

19. The method of Claim 18 wherein a capacitance ratio of said capacitor of said Ahuja compensation circuit to said Miller compensation capacitor is less than about 3.

20. The method of Claim 18 wherein said zero frequency is within a factor of 4 of said pole frequency.

21. The method of Claim 18 said zero and said pole are within a factor of $(1+C_a/C_m)$.

22. A voltage regulator, comprising:

error amplifying means for amplifying a voltage difference between a reference voltage and a sampled output voltage of the voltage regulator;

driver amplifying means for receiving said amplified voltage difference and for producing a gate driving voltage;

output means for receiving said gate driving voltage and for generating a regulated output voltage;

first compensation means for feeding a sample of said regulated output voltage back to an input of said driver amplifying means; and

second compensation means for feeding back a portion of said regulated output voltage back to said input of said driver amplifying means.

23. The voltage regulator of Claim 22 wherein a zero resulting from said first compensation means at least partially cancels a pole resulting from said second compensation means.

24. The voltage regulator of Claim 23 wherein said zero produced by said first compensation means tracks said pole produced by said second compensation means.

25. The voltage regulator of Claim 23 wherein a frequency of said zero produced by said first compensation means is within a factor of (1+Ca/Cm) of a frequency of said pole produced by said second compensation means.

26. The voltage regulator of Claim 23 wherein said second compensation means includes an Ahuja feedback capacitor and said first compensation means includes a Miller compensation capacitor, and wherein a ratio of said Ahuja feedback capacitor and said Miller compensation capacitor is less than about 3.

27. The voltage regulator of Claim 22 wherein said driver amplifying means has an output impedance of between about 100Ω and 200Ω.

28. The voltage regulator of Claim 22 wherein said driver amplifying means comprises a plurality of series-connected amplifiers.

29. The voltage regulator of Claim 28 wherein said driver amplifying means comprises four series-connected amplifiers.

30. The voltage regulator of Claim 29 wherein said voltage regulator includes at least two nested feedback paths.

31. The voltage regulator of Claim 22 wherein said error amplifying means comprises a P-channel input differential pair amplifier.

32. The voltage regulator of Claim 22 wherein said output means is a power P-channel MOSFET.

33. A method for operating a voltage regulator, comprising:

amplifying a voltage difference between a reference and a sampled output voltage of the voltage regulator;

producing a gate driving voltage based on said amplified voltage difference;

receiving said gate driving voltage and outputting a regulated output voltage;

feeding back a sample of said regulated output voltage to provide Miller compensation; and

feeding back a portion of said regulated output voltage to provide Ahuja compensation.

34. The method of Claim 33 further comprising partially canceling a zero produced by said Miller compensation using a pole produced by said Ahuja compensation.

35. The method of Claim 34 wherein said zero produced by said Miller compensation tracks said pole produced by said Ahuja compensation.

36. The method of Claim 34 wherein a frequency of said zero produced by said Miller compensation is within a factor of (1+Ca/Cm) of a frequency of said pole produced by said Ahuja compensation.